

Notice of References Cited	Application/Control No. 10/768,401	Applicant(s)/Patent Under Reexamination BORGATTI ET AL.	
	Examiner Eric Coleman	Art Unit 2183	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Brown, S., and J. Rose, FPGA and CPLD Architectures: A Tutorial. IEEE Design and Test of Computers, 1996, pp. 42-57.
	V	Eclipse-II FPGAs for Low Power Applications QuickLogic White paper, QuickLogic Corporation, 2003 pp. 1-7.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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